Paper No. 42

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MASAHARU HAMASAKI

Appeal No. 1998-2483
Application No. 08/289,347

HEARD: January 23, 2001

Before KRASS, DIXON, and BLANKENSHIP, **Administrative Patent Judges**.

DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claim 10, which is the only claim pending in this application.

We REVERSE.

BACKGROUND

The appellant's invention relates to a method of manufacturing a semiconductor device using high energy ion implantation and high heat to diffuse the implanted ions. An understanding of the invention can be derived from a reading of exemplary claim 10, which is reproduced below.

> 10. A method of manufacturing an interline CCD image sensor, the method comprising the steps of:
>
> providing a semiconductor substrate of a first conductivity type;
>
> ion-implanting impurities directly into the semiconductor substrate which is free of any layer at an energy of 0.7 to 16 MeV;
>
> heat-treating the implanted impurities for a period in which a diffusion time calculated in terms of 1100°C is less than 10 hours so as to form a well of a second conductivity type in the semiconductor substrate; and
>
> forming an image sensing section and a vertical transfer channel in a surface of the well wherein the well is formed such that a peak of an impurity concentration is located at a deep position from the substrate surface so that a relatively lower impurity concentration region is formed on the surface thereby to reduce residual image and blooming of the image sensor.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Odanaka	5,160,996	Nov. 03, 1992

Pramanik et al.(Pramanik), “MeV Implantation for Silicon Device Fabrication,” Solid State Technology, pp. 211-216, May 1984.

Admitted Prior Art at pages 1-2 of the specification (APA).

Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Pramanik in view of APA. Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Odanaka in view of APA.

Rather than reiterate the conflicting viewpoints advanced by the examiner and the appellant regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 38, mailed April 14, 1998) for the examiner's reasoning in support of the rejections, and to the appellant's brief (Paper No. 37, filed January 20, 1998) for the appellant's arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellant's specification and claims, to the applied prior art references, and to the respective positions articulated by the appellant and the examiner. As a consequence of our review, we make the determinations which follow.

Appellant argues that both Pramanik and Odanaka teach CMOS devices rather than the interlining CCD of the present claims and that the characteristic problems of a

CCD are not existent in CMOS devices. (See brief at page 9.) Appellant argues that the prior art to Pramanik and Odanaka does not teach the claim limitation of "forming an image sensing section and a vertical transfer channel in a surface of the well wherein the well is formed such that a peak of an impurity concentration is located at a deep position from the substrate surface so that a relatively lower impurity concentration region is formed on the surface thereby to reduce residual image and blooming of the image sensor." (See brief at page 9.) We agree with appellant that the prior art references to Pramanik and Odanaka do not teach this limitation.

The examiner relies upon appellant's statement in the specification that wells are used in both CMOS and CCD's. (See specification at page 1.) (See answer at page 4.) Appellant further states that the wells are formed in the prior art by selectively diffusing impurities into the surface of a semiconductor substrate and the problems associated therewith. (See specification at pages 1-2). The examiner relies upon appellant's statement of the problem with deep wells and that therefore, it would be obvious to use the disclosed process used for CMOS for the CCD's also. With the obviousness of the process, the varied concentration of the impurities would have been "inherent" and that residual image and blooming of the image sensor would be reduced. We disagree with the examiner. This is merely speculation on the part of the

examiner without any statement of support in the prior art references or any support in the brief statements in appellant's specification.

Appellant argues that the admitted prior art does not show the peak concentration of impurities at a deep position from the substrate surface. (See brief at page 9.) We agree with appellant. Appellant argues that the admitted prior art Figure 3 does not show that the impurity concentration of the prior art device which has the concentration on the surface cannot be lowered as compared with the peak concentration of the well. Therefore, it would not be inherent that the residual image blooming of the image sensor is reduced as the examiner contends. (See brief at page 10 and 11.) We agree with appellant.

When relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. **See Ex parte Levy**, 17 USPQ2d 1461, 1464 (Bd. Patent App. & Int. 1990)(discussing inherency as it relates to a rejection based upon anticipation). Here, we find that the examiner has not provided any basis for the speculative conclusion that the residual image blooming of the image sensor would be reduced.

Therefore, the examiner has not established a ***prima facie*** case of obviousness of the invention as recited in the language of claim 10, and we cannot sustain the rejection of claim 10.

CONCLUSION

To summarize, the decision of the examiner to reject claim 10 under 35 U.S.C. § 103(a) is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)
JOSEPH L. DIXON Administrative Patent Judge	) BOARD OF PATENT) APPEALS) AND) INTERFERENCES
HOWARD B. BLANKENSHIP Administrative Patent Judge	)

jld/vsh

SONNENSCHEIN, NATH & ROSENTHAL
P.O. BOX 061080
WACKER DRIVE STATION
SEARS TOWER
CHICAGO, IL 60606-1080